UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,943	08/30/2001	Woo-sik Eom	1293.1231	6347

21171 7590 09/28/2005

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,943	EOM, WOO-SIK	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17-27 and 29-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17-27 and 29-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claim 39 has been added. Claims 1-15, 17-27 and 29-38 are pending and under consideration. Claims 1-15, 17-27 and 29-39 have been examined.

Specification

2. The disclosure is objected to because of the description of the block boundary signal as a mono multi-pulse signal is not clear. There is not description in the specification as to what a mono multi-pulse signal is. Figure 3A is insufficient. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 39 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 39:

The claim limitation "the boundary block signal is a mono multi-pulse signal" renders the claim indefinite. The Examiner is not sure what is meant by "a mono multi-pulse signal" and paragraph 28 in the specification does define in such a way that the Examiner knows explicitly what the Applicant means.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-13, 19-24 and 33-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Owa et al. (US-6564009), hereinafter Owa.

Claim 1:

Owa teaches that a frame address detecting circuit 137 (decoder) receives the push pull signal PP outputted from the optical head 11 and samples a wobble signal (ECC block) by a built-in band-pass filter (block address information recorded on the disk). Owa also teaches the frame address detecting circuit 137 may decode the wobble data ADIP (ECC block) by detecting a change in the phase of the wobble signal (detecting a phase difference) and executing predetermined signal processing and may output the decoded wobble data ADIP (generating a block boundary signal) to a system control circuit 134 and the cluster counter 138. (Col. 41, lines 6-17, Fig. 42). Owa further teaches the recording and reproducing circuit 53 forms an ECC data block (182 bytes X 208 bytes) by 16 of the sector data blocks (encoder adding an error correction code). Owa even further teaches, the recording and reproducing circuit 53 interleaves the ECC

block and form a frame structure shown by FIG. 14 and allocates a frame synchronizing signal (FS) (encoding block synchronous signal) of 2 bytes to each 91 bytes of the ECC data block of 182 bytes X 208 bytes thereby forming 412 frames by one ECC data block. (Col. 18, lines 50-64, Fig. 13). Owa discloses in PLL circuit 135, a binarized signal outputted from the wobbling period detecting circuit 40 (encoding block synchronous signal) is provided to a phase comparing circuit (PC) 135A where the binarized signal may be compared with the clock CK outputted from a dividing circuit 135B with regard to the phase (detecting a phase difference). Owa also discloses that the frame address detecting circuit 137 performs error detection processing carried out by error detection code CRCC allocated to each address data frame and the wobble data ADIP outputted after removing an error detection code and a reserve bit from the wobble data which has been determined correct (detecting whether a violation of the boundary occurs). (Col. 41, lines 21-31, Fig. 42).

Claims 19 and 33:

Owa teaches that a frame address detecting circuit 137 (decoder) receives the push pull signal PP outputted from the optical head 11 and samples a wobble signal (ECC block) by a built-in band-pass filter (block address information recorded on the disk). Owa also teaches the frame address detecting circuit 137 may decode the wobble data ADIP (ECC block) by detecting a change in the phase of the wobble signal (detecting inconsistencies/determining a phase difference) and executing predetermined signal processing and may output the decoded wobble data ADIP (generating a block boundary signal) to a system control circuit 134 and the cluster

counter 138. (Col. 41, lines 6-17, Fig. 42). Owa further teaches the recording and reproducing circuit 53 forms an ECC data block (182 bytes X 208 bytes) by 16 of the sector data blocks (encoder adding an error correction code). Owa even further teaches, the recording and reproducing circuit 53 interleaves the ECC block and form a frame structure shown by FIG. 14 and allocates a frame synchronizing signal (FS) (encoding block synchronous signal) of 2 bytes to each 91 bytes of the ECC data block of 182 bytes X 208 bytes thereby forming 412 frames by one ECC data block. (Col. 18, lines 50-64, Fig. 13). Owa discloses in PLL circuit 135, a binarized signal outputted from the wobbling period detecting circuit 40 (encoding block synchronous signal) is provided to a phase comparing circuit (PC) 135A where the binarized signal may be compared with the clock CK outputted from a dividing circuit 135B with regard to the phase (detecting inconsistencies/determining a phase difference). Owa also discloses that the frame address detecting circuit 137 performs error detection processing carried out by error detection code CRCC allocated to each address data frame and the wobble data ADIP outputted after removing an error detection code and a reserve bit from the wobble data which has been determined correct (detecting whether a violation of the boundary occurs). (Col. 41, lines 21-31, Fig. 42).

Claim 21:

Owa teaches that a frame address detecting circuit 137 (decoder) receives the push pull signal PP outputted from the optical head 11 and samples a wobble signal (ECC block) by a built-in band-pass filter (block address information recorded on the disk). Owa also teaches the frame address detecting circuit 137 (decoder) may decode

the wobble data ADIP (ECC block) by detecting a change in the phase of the wobble signal (detecting a phase difference) and executing predetermined signal processing and may output the decoded wobble data ADIP (generating a block boundary signal) to a system control circuit 134 and the cluster counter 138. (Col. 41, lines 6-17, Fig. 42). Owa further teaches the recording and reproducing circuit 53 (encoder) forms an ECC data block (182 bytes X 208 bytes) by 16 of the sector data blocks (encoder adding an error correction code). Owa even further teaches, the recording and reproducing circuit 53 (encoder) interleaves the ECC block and form a frame structure shown by FIG. 14 and allocates a frame synchronizing signal (FS) (encoding block synchronous signal) of 2 bytes to each 91 bytes of the ECC data block of 182 bytes X 208 bytes thereby forming 412 frames by one ECC data block. (Col. 18, lines 50-64, Fig. 13). Owa discloses in PLL circuit 135, a binarized signal outputted from the wobbling period detecting circuit 40 (encoding block synchronous signal) is provided to a phase comparing circuit (PC) 135A where the binarized signal may be compared with the clock CK outputted from a dividing circuit 135B with regard to the phase (detecting a phase difference). Owa also discloses that the frame address detecting circuit 137 performs error detection processing carried out by error detection code CRCC allocated to each address data frame and the wobble data ADIP outputted after removing an error detection code and a reserve bit from the wobble data which has been determined correct (detecting whether a violation of the boundary occurs). (Col. 41, lines 21-31, Fig. 42).

Claim 2:

Owa teaches a comparing circuit (COM) 183 binarizes the wobble signal WB with regard to a 0 level so as to form a binarized signal S2 in which edge information is detected or obtained from the wobble signal WB (FIGS. 52A through 52D) (generating a window signal indicative of a recording allowable range based on the block boundary signal) whereas either a rising edge or a falling edge of the binarized signal S2 is provided with correct phase information and phase information of the remaining or other edge corresponds with information of the wobble data ADIP. Owa also teaches a phase comparing circuit (PC) 184 which may include constituted by an EXCLUSIVE OR circuit (performing a logic operation on the window signal) compares phases of the wobble clock WCK and the wobble signal WB and outputs a result SCOM of such phase comparison (FIGS. 52D through 52G). (Col. 45, lines 26-44).

Claim 3:

Owa teaches the wobble signal processing circuit 173 reproduces the wobble data ADIP by effectively utilizing the following relationship where a counter (CNT) 189 clears a count value with a rise edge of the binarized signal S2 as a reference, counts up the reading/writing clock R/W CK during a time period where the logical level of the binarized signal S2 rises and counts down the reading/writing clock R/W CK during the time period where the logical level of the binarized signal S2 falls (FIGS. 53A through 53F) (generating window signals). Owa goes on to teach the counter 189 detects an advance phase (leads a phase) and a retard phase (lags the phase) of the wobble signal WB (encoding signal) in respect of the wobble clock WCK by the count value

CNT with a half period of the wobble data ADIP as a unit. Owa also teaches a flip flop (FF) 190 retards the count value CNT by the half period of the wobble data ADIP. Owa further teaches a subtracting circuit 191 subtracts output data of the counter 189 from the output data of the flip flop 190 (performing a logic operation on the window signals) and detects a change in timing where the wobble signal WB carries out zero crossing before and after the respective references of a bit boundary and bit center of the wobble data ADIP. When the timing change is advanced (leads) in respect of the wobble clock WCK, the subtraction result is a negative value L2 which is twice the count value CNT. When the timing change is retarded (lags) in respect of the wobble clock WCK, the subtraction result is a positive value H2 that is twice the count value CNT. When the phase remains unchanged, the subtraction result is a value 0 (FIG. 53G). (Col. 46, lines 19-44).

Claim 4 and 24:

Owa teaches although embodiments have been described wherein a magneto-optical disk, a phase change type optical disk and a write once type optical disk may be used in one optical disk device, the present invention is not limited thereto and may be applied to other arrangements such as where only one kind of an optical disk is used in an optical disk device or where a DVD, compact disk or the like in addition to optical disks is used in an optical disk device (the disk is one of a DVD-R disk, a DVD-RW disk, a DVD+RW disk, a CD-R disk, and a CD-RW disk). (Col. 48, lines 64-67, col. 49, lines 1-4).

Claim 5:

Owa even further teaches, the recording and reproducing circuit 53 interleaves the ECC block and form a frame structure shown by FIG. 14 and allocates a frame synchronizing signal (FS) (generating of the block boundary signal uses block address information of the ECC blocks recorded on the disk) of 2 bytes to each 91 bytes of the ECC data block of 182 bytes X 208 bytes thereby forming 412 frames by one ECC data block. (Col. 18, lines 50-64, Fig. 13).

Claim 6:

Owa teaches although embodiments have been described wherein a magneto-optical disk, a phase change type optical disk and a write once type optical disk may be used in one optical disk device, the present invention is not limited thereto and may be applied to other arrangements such as where only one kind of an optical disk is used in an optical disk device or where a DVD, compact disk or the like in addition to optical disks is used in an optical disk device (the disk is one of a DVD-R disk, a DVD-RW disk, a DVD+RW disk, a CD-R disk, and a CD-RW disk). (Col. 48, lines 64-67, col. 49, lines 1-4). Owa also teaches when an optical disk is fabricated from the original disk 2, the laser beam L may be irradiated such that widths of a groove (ADIP) and a land (land of the disk) are substantially equal. (Col. 39, lines 10-12).

Claim 7:

Owa teaches the recording and reproducing circuit 53 forms an ECC data block and interleaves the ECC block and form a frame structure shown by FIG. 14 and allocates a frame synchronizing signal (FS). (Col. 18, lines 50–67). Owa also teaches

frame address circuit 137 decodes the wobble data ADIP (address information of the ECC blocks is recorded as a wobble signal). (Col. 41, lines 12, 13).

Claim 8:

Owa teaches the link frames are used for buffers between contiguous clusters in recording data to the optical disk 11 a cluster unit(s), as shown by FIG. 46, with the optical disk device 110, after recording 56 bytes of data and 3 link frames successively to the optical disk 112, frames constituted by ECC blocks are successively recorded (normally recording in response to the phase of the block boundary signal being consistent with the phase of the encoding block synchronous signal). (Col. 42, lines 52-57).

Claim 9:

Owa teaches the link frames are used for buffers between contiguous clusters in recording data to the optical disk 11 a cluster unit(s), as shown by FIG. 46, with the optical disk device 110, after recording 56 bytes of data and 3 link frames successively to the optical disk 112, frames constituted by ECC blocks are successively recorded (normally recording comprises recording the encoding block from the boundaries between the ECC blocks on the disk). (Col. 42, lines 52-57).

Claim 10:

Owa teaches the recording and reproducing circuit 53 may set the redundancy to 23(%) or less and may efficiently record the user data by adding redundant data such as the frame synchronizing signal, error correction code, the frame address and so on to the user data (performing an error correction to provide for a margin of error between

a phase of the block boundary signal and a phase of the encoding block synchronous signal). (Col. 19, lines 1-5).

Claim 11:

Owa teaches the recording and reproducing circuit 53 may set the redundancy to 23(%) or less and may efficiently record the user data by adding redundant data such as the frame synchronizing signal, error correction code, the frame address and so on to the user data (determining whether a phase of the block boundary signal is consistent with a phase of the encoding block synchronous signal within a window signal having a width determined by considering a margin of error). (Col. 19, lines 1-5).

Claim 12 and 13:

Owa teaches the system control circuit 34 may interrupt recording to the optical disk 12 (generating an interrupt signal) when the amount of the user data held in the memory 54 is a predetermined value or less (the phase of the block boundary signal being inconsistent with the phase of the encoding block synchronous signal). (Col. 22, lines 17-19).

Claims 20 and 34:

Owa teaches that a frame address detecting circuit 137 (decoder) receives the push pull signal PP outputted from the optical head 11 and samples a wobble signal (ECC block) by a built-in band-pass filter (receiving a signal from the disk and generating a block boundary signal). (Col. 41, lines 6-17, Fig. 42). Owa also teach the counter 189 detects an advance phase (generating a first window...leads a phase) and a retard phase (generating a third window...lags the phase) of the wobble signal WB

(encoding signal) in respect of the wobble clock WCK by the count value CNT with a half period of the wobble data ADIP as a unit. (Col. 46, lines 19-44). Owa further teaches a comparing circuit (COM) 183 binarizes the wobble signal WB with regard to a 0 level so as to form a binarized signal S2 in which edge information is detected or obtained from the wobble signal WB (FIGS. 52A through 52D) (generating a second window signal detecting whether the block boundary signal and the encoding block synchronous signal exist within a range) whereas either a rising edge or a falling edge of the binarized signal S2 is provided with correct phase information and phase information of the remaining or other edge corresponds with information of the wobble data ADIP. (Col. 45, lines 26-44). Owa discloses a flip flop (FF) 190 retards the count value CNT by the half period of the wobble data ADIP (encoding block synchronous signal). Owa also discloses a subtracting circuit 191 subtracts output data of the counter 189 from the output data of the flip flop 190 and detects a change in timing where the wobble signal WB carries out zero crossing before and after the respective references of a bit boundary and bit center of the wobble data ADIP. Owa further discloses when the timing change is advanced (comparing the encoding block synchronous signal with the first window signal) in respect of the wobble clock WCK, the subtraction result is a negative value L2 which is twice the count value CNT. Owa even further discloses when the timing change is retarded (comparing the encoding block synchronous signal with the third window signal) in respect of the wobble clock WCK, the subtraction result is a positive value H2 that is twice the count value CNT. When the phase remains unchanged, the subtraction result is a value 0 (FIG. 53G). (Col. 46, lines 19-44). Owa

also teaches a phase comparing circuit (PC) 184 which may include constituted by an EXCLUSIVE OR circuit (comparing the encoding block synchronous signal with the second window signal) compares phases of the wobble clock WCK and the wobble signal WB and outputs a result SCOM of such phase comparison (FIGS. 52D through 52G). (Col. 45, lines 26-44).

Claim 22:

Owa teach the counter 189 detects an advance phase (a first window generator ...leads a phase) and a retard phase (a third window generator ...lags the phase) of the wobble signal WB (encoding block) in respect of the wobble clock WCK by the count value CNT with a half period of the wobble data ADIP as a unit. (Col. 46, lines 19-44). Owa also teaches a flip flop (FF) 190 retards the count value CNT by the half period of the wobble data ADIP. Owa further teaches a subtracting circuit 191 subtracts output data of the counter 189 from the output data of the flip flop 190 (a first logic gate and a third logic gate performing a logic operation on the first window signal, the third window signal...) and detects a change in timing where the wobble signal WB carries out zero crossing before and after the respective references of a bit boundary and bit center of the wobble data ADIP. When the timing change is advanced (leads) in respect of the wobble clock WCK, the subtraction result is a negative value L2 which is twice the count value CNT. When the timing change is retarded (lags) in respect of the wobble clock WCK, the subtraction result is a positive value H2 that is twice the count value CNT. When the phase remains unchanged, the subtraction result is a value 0 (FIG. 53G). (Col. 46, lines 19-44).

Claim 23:

Owa teaches a comparing circuit (COM) 183 binarizes the wobble signal WB with regard to a 0 level so as to form a binarized signal S2 in which edge information is detected or obtained from the wobble signal WB (FIGS. 52A through 52D) (a second window signal generator generating a second window signal indicative of the recording allowable range based on the block boundary signal) whereas either a rising edge or a falling edge of the binarized signal S2 is provided with correct phase information and phase information of the remaining or other edge corresponds with information of the wobble data ADIP. Owa also teaches a phase comparing circuit (PC) 184 which may include constituted by an EXCLUSIVE OR circuit (a second logic gate performing a logic operation on the second window signal and the encoding block synchronous signal...) compares phases of the wobble clock WCK and the wobble signal WB and outputs a result SCOM of such phase comparison (FIGS. 52D through 52G). (Col. 45, lines 26-44).

Claim 35:

Owa teaches the recording and reproducing circuit 53 forms an ECC data block (182 bytes X 208 bytes) by 16 of the sector data blocks (adding an error correction code). Owa also teaches, the recording and reproducing circuit 53 (encoder) interleaves the ECC block and form a frame structure shown by FIG. 14 and allocates a frame synchronizing signal (FS) (generating the encoding block) of 2 bytes to each 91 bytes of the ECC data block of 182 bytes X 208 bytes thereby forming 412 frames by one ECC

data block (outputting the encoding block with the ecoding block synchronous signal). (Col. 18, lines 50-64, Fig. 13).

Claim 36:

Owa teaches the counter 189 detects an advance phase (the first window signal continues from a middle of a previous ECC block to a start of the second window signal) and a retard phase (the third window signal continues from an end of the second window signal to a middle of a next ECC block) of the wobble signal WB (encoding signal) in respect of the wobble clock WCK by the count value CNT with a half period of the wobble data ADIP as a unit. (Col. 46, lines 19-44). Owa also teaches a comparing circuit (COM) 183 binarizes the wobble signal WB with regard to a 0 level so as to form a binarized signal S2 in which edge information is detected or obtained from the wobble signal WB (FIGS. 52A through 52D) (the second window signal comprises a width determined by considering a margin on the basis of the block boundary signal) whereas either a rising edge or a falling edge of the binarized signal S2 is provided with correct phase information and phase information of the remaining or other edge corresponds with information of the wobble data ADIP. (Col. 45, lines 26-44).

Claim 37:

Owa teaches that a frame address detecting circuit 137 (decoder) receives the push pull signal PP outputted from the optical head 11 and samples a wobble signal (ECC block) by a built-in band-pass filter (generates a pulse for each boundary between blocks). Owa also teaches the frame address detecting circuit 137 (decoder) may decode the wobble data ADIP (ECC block) by detecting a change in the phase of the

wobble signal and executing predetermined signal processing and may output the decoded wobble data ADIP (outputs the pulse as the block boundary signal) to a system control circuit 134 and the cluster counter 138. (Col. 41, lines 6-17, Fig. 42). Owa further teaches the wobble signal generating circuit 107 (also part of the decoder) is adapted to form a wobble signal WB from the wobble data ADIP or the like (LPP). (Col. 39, lines 66, 67).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 14, 25, 26, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owa et al. (US-6564009), hereinafter Owa.

Claim 14, 25, 26, and 38:

Owa does not explicitly teach the logic operation (or first, second, and third logic gates) are performed by AND gates. However, Owa does suggest a phase comparing circuit (PC) 184 which may include constituted by an EXCLUSIVE OR circuit and a subtracting circuit 191 subtracts output data of the counter 189 from the output data of the flip flop 190 and detects a change in timing where the wobble signal WB carries out zero crossing before and after the respective references of a bit boundary and bit center of the wobble data ADIP. (Col 45, lines 39-44, Col. 46, lines 32-38). It would have been

obvious to one of ordinary skill in the art at the time the invention was made the Owa's phase comparing circuit (PC) 184 could comprise of AND gates to perform the comparison function. The artisan would have been motivated to do so because then Owa would have an alternate logical combination for possible critical path timing in the comparison signal. It also would have been obvious to one of ordinary skill in the art at the time the invention was made to use AND gates in the subtracting circuit 191 because it is well known in the art that subtracting circuits include AND functions.

6. Claims 15, 17, 18, 27, 29-32, and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Owa et al. (US-6564009), hereinafter Owa in view of Ueki (US-6678236).

Claims 15 and 27:

Owa teaches that a frame address detecting circuit 137 (decoder) receives the push pull signal PP outputted from the optical head 11 and samples a wobble signal (ECC block) by a built-in band-pass filter (block address information recorded on the disk). Owa also teaches the frame address detecting circuit 137 may decode the wobble data ADIP (ECC block) by detecting a change in the phase of the wobble signal (detecting inconsistencies/determining a phase difference) and executing predetermined signal processing and may output the decoded wobble data ADIP (generating a block boundary signal) to a system control circuit 134 and the cluster counter 138. (Col. 41, lines 6-17, Fig. 42). Owa further teaches the recording and reproducing circuit 53 forms an ECC data block (182 bytes X 208 bytes) by 16 of the

sector data blocks (encoder adding an error correction code). Owa even further teaches, the recording and reproducing circuit 53 interleaves the ECC block and form a frame structure shown by FIG. 14 and allocates a frame synchronizing signal (FS) (encoding block synchronous signal) of 2 bytes to each 91 bytes of the ECC data block of 182 bytes X 208 bytes thereby forming 412 frames by one ECC data block. (Col. 18, lines 50-64, Fig. 13). Owa discloses in PLL circuit 135, a binarized signal outputted from the wobbling period detecting circuit 40 (encoding block synchronous signal) is provided to a phase comparing circuit (PC) 135A where the binarized signal may be compared with the clock CK outputted from a dividing circuit 135B with regard to the phase (detecting inconsistencies/determining a phase difference). Owa also discloses that the frame address detecting circuit 137 performs error detection processing carried out by error detection code CRCC allocated to each address data frame and the wobble data ADIP outputted after removing an error detection code and a reserve bit from the wobble data which has been determined correct (detecting whether a violation of the boundary occurs). (Col. 41, lines 21-31, Fig. 42).

Owa teaches that a frame address detecting circuit 137 (decoder) receives the push pull signal PP outputted from the optical head 11 and samples a wobble signal (ECC block) by a built-in band-pass filter (receiving a signal from the disk and generating a block boundary signal). (Col. 41, lines 6-17, Fig. 42). Owa also teach the counter 189 detects an advance phase (generating a first window...leads a phase) and a retard phase (generating a third window...lags the phase) of the wobble signal WB (encoding signal) in respect of the wobble clock WCK by the count value CNT with a

half period of the wobble data ADIP as a unit. (Col. 46, lines 19-44). Owa further teaches a comparing circuit (COM) 183 binarizes the wobble signal WB with regard to a 0 level so as to form a binarized signal S2 in which edge information is detected or obtained from the wobble signal WB (FIGS. 52A through 52D) (generating a second window signal detecting whether the block boundary signal and the encoding block synchronous signal exist within a range) whereas either a rising edge or a falling edge of the binarized signal S2 is provided with correct phase information and phase information of the remaining or other edge corresponds with information of the wobble data ADIP. (Col. 45, lines 26-44). Owa discloses a flip flop (FF) 190 retards the count value CNT by the half period of the wobble data ADIP (encoding block synchronous signal). Owa also discloses a subtracting circuit 191 subtracts output data of the counter 189 from the output data of the flip flop 190 and detects a change in timing where the wobble signal WB carries out zero crossing before and after the respective references of a bit boundary and bit center of the wobble data ADIP. Owa further discloses when the timing change is advanced (comparing the encoding block synchronous signal with the first window signal) in respect of the wobble clock WCK, the subtraction result is a negative value L2 which is twice the count value CNT. Owa even further discloses when the timing change is retarded (comparing the encoding block synchronous signal with the third window signal) in respect of the wobble clock WCK, the subtraction result is a positive value H2 that is twice the count value CNT. When the phase remains unchanged, the subtraction result is a value 0 (FIG. 53G). (Col. 46, lines 19-44). Owa also teaches a phase comparing circuit (PC) 184 which may include constituted by an

EXCLUSIVE OR circuit (comparing the encoding block synchronous signal with the second window signal) compares phases of the wobble clock WCK and the wobble signal WB and outputs a result SCOM of such phase comparison (FIGS. 52D through 52G). (Col. 45, lines 26-44).

Owa does not explicitly disclose the use of interrupts. However, Owa does teach a recording and reproducing circuit 53 may store the user data DU outputted from the encoder 51 to a memory 54 in recording and editing and may record the user data DU to the optical disk 12 by processing it by a predetermined block unit, that is, as shown by FIG. 12, the recording and reproducing circuit 53 may successively block the user data DU (a type of recording interrupt function) in a unit having 2048 bytes and may add address data and error detection code having 16 bytes to each block. Owa also teaches the recording and reproducing circuit 53 may interleave the ECC block and form a frame structure shown by FIG. 14. That is, the recording and reproducing circuit 53 may allocate a frame synchronizing signal (FS) of 2 bytes to each 91 bytes of the ECC data block of 182 bytes X 208 bytes thereby forming 412 frames by one ECC data block. (Col. 18, ll. 40-44, 59-64). Ueki teaches in an analogous art with reference to FIG. 15, a first portion of the 1-ECC-block data is recorded while the LPP-based recording timing signal is used as reference timings indicative of the boundaries between sectors or the heads of sectors. Ueki also teaches at the timing corresponding to the starting edge of the pre-pit area PR and given by the LPP-based recording timing signal, the system controller 9 suspends the recording (**recording interrupt**) and changes the operation of the apparatus from the recording mode to the playback mode. (Col. 26, ll. 45-55). It

would have been obvious to one of ordinary skill in the art at the time the invention was made modify Owa's recording and reproducing circuit 53 with the suspends recording function (recording interrupt) of Ueki's system controller 9. The artisan would have been motivated to do so because this would allow Owa to have better control on interrupting the recording and playback modes based on the comparison of the pre-pit area PR and the LPP-based recording timing signal.

Claims 17 and 29:

Owa teaches the recording and reproducing circuit 53 forms an ECC data block (182 bytes X 208 bytes) by 16 of the sector data blocks (adding an error correction code). Owa also teaches, the recording and reproducing circuit 53 (encoder) interleaves the ECC block and form a frame structure shown by FIG. 14 and allocates a frame synchronizing signal (FS) (generating the encoding block) of 2 bytes to each 91 bytes of the ECC data block of 182 bytes X 208 bytes thereby forming 412 frames by one ECC data block (outputting the encoding block with the ecoding block synchronous signal). (Col. 18, lines 50-64, Fig. 13).

Claims 18 and 30:

Owa teaches the counter 189 detects an advance phase (the first window signal continues from a middle of a previous ECC block to a start of the second window signal) and a retard phase (the third window signal continues from an end of the second window signal to a middle of a next ECC block) of the wobble signal WB (encoding signal) in respect of the wobble clock WCK by the count value CNT with a half period of the wobble data ADIP as a unit. (Col. 46, lines 19-44). Owa also teaches a comparing

circuit (COM) 183 binarizes the wobble signal WB with regard to a 0 level so as to form a binarized signal S2 in which edge information is detected or obtained from the wobble signal WB (FIGS. 52A through 52D) (the second window signal comprises a width determined by considering a margin on the basis of the block boundary signal) whereas either a rising edge or a falling edge of the binarized signal S2 is provided with correct phase information and phase information of the remaining or other edge corresponds with information of the wobble data ADIP. (Col. 45, lines 26-44).

Claim 31:

Owa teaches that a frame address detecting circuit 137 (decoder) receives the push pull signal PP outputted from the optical head 11 and samples a wobble signal (ECC block) by a built-in band-pass filter (generates a pulse for each boundary between blocks). Owa also teaches the frame address detecting circuit 137 (decoder) may decode the wobble data ADIP (ECC block) by detecting a change in the phase of the wobble signal and executing predetermined signal processing and may output the decoded wobble data ADIP (outputs the pulse as the block boundary signal) to a system control circuit 134 and the cluster counter 138. (Col. 41, lines 6-17, Fig. 42). Owa further teaches the wobble signal generating circuit 107 (also part of the decoder) is adapted to form a wobble signal WB from the wobble data ADIP or the like (LPP). (Col. 39, lines 66, 67).

Claim 32:

Owa does not explicitly teach the logic operation (or first, second, and third logic gates) are performed by AND gates. However, Owa does suggest a phase comparing

circuit (PC) 184 which may include constituted by an EXCLUSIVE OR circuit and a subtracting circuit 191 subtracts output data of the counter 189 from the output data of the flip flop 190 and detects a change in timing where the wobble signal WB carries out zero crossing before and after the respective references of a bit boundary and bit center of the wobble data ADIP. (Col 45, lines 39-44, Col. 46, lines 32-38). It would have been obvious to one of ordinary skill in the art at the time the invention was made the Owa's phase comparing circuit (PC) 184 could comprise of AND gates to perform the comparison function. The artisan would have been motivated to do so because then Owa would have an alternate logical combination for possible critical path timing in the comparison signal. It also would have been obvious to one of ordinary skill in the art at the time the invention was made to use AND gates in the subtracting circuit 191 because it is well known in the art that subtracting circuits include AND functions.

Claim 39:

Owa teaches that a frame address detecting circuit 137 (decoder) receives the push pull signal PP outputted from the optical head 11 and samples a wobble signal (ECC block) by a built-in band-pass filter (block address information recorded on the disk). Owa also teaches the frame address detecting circuit 137 may decode the wobble data ADIP (ECC block) by detecting a change in the phase of the wobble signal (detecting a phase difference) and executing predetermined signal processing and may output the decoded wobble data ADIP (generating a block boundary signal) to a system control circuit 134 and the cluster counter 138. (Col. 41, lines 6-17, Fig. 42). Owa further teaches the recording and reproducing circuit 53 forms an ECC data block (182 bytes X

208 bytes) by 16 of the sector data blocks (encoder adding an error correction code). Owa even further teaches, the recording and reproducing circuit 53 interleaves the ECC block and form a frame structure shown by FIG. 14 and allocates a frame synchronizing signal (FS) (encoding block synchronous signal) of 2 bytes to each 91 bytes of the ECC data block of 182 bytes X 208 bytes thereby forming 412 frames by one ECC data block. (Col. 18, lines 50-64, Fig. 13). Owa discloses in PLL circuit 135, a binarized signal outputted from the wobbling period detecting circuit 40 (encoding block synchronous signal) is provided to a phase comparing circuit (PC) 135A where the binarized signal may be compared with the clock CK outputted from a dividing circuit 135B with regard to the phase (detecting a phase difference). Owa also discloses that the frame address detecting circuit 137 performs error detection processing carried out by error detection code CRCC allocated to each address data frame and the wobble data ADIP outputted after removing an error detection code and a reserve bit from the wobble data which has been determined correct (detecting whether a violation of the boundary occurs). (Col. 41, lines 21-31, Fig. 42).

Owa does not explicitly disclose "the block boundary signal is a mono multi-pulse signal generated at the boundary between the ECC blocks". However, Owa does teach In the wobble signal generating circuit 107, wobble data ADIP (ECC block) may be subjected to biphase mark modulation (FIGS. 41A and 41B) (generating a block boundary signal). Owa also teaches synchronization patterns may be inserted, the phase modulating signal having a single carrier frequency may be formed and the

phase modulating signal may be outputted as the wobble signal WB (FIG. 41C). (Col. 18, ll. 59-64).

Ueki teaches in an analogous art a mono multi-pulse signal generated at the boundary between the ECC blocks with reference to FIG. 15, in that a first portion of the 1-ECC-block data is recorded while the LPP-based recording timing signal (block boundary signal is a mono multi-pulse signal) is used as reference timings indicative of the boundaries between sectors or the heads of sectors. (Col. 26, ll. 45-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made modify Owa's wobble signal generating circuit 107 so the inserted synchronization patterns is generated as a mono multi-pulse signal Ueki's LPP-based recording timing signal. The artisan would have been motivated to do so because this would allow Owa to better define the block boundary of the ECC blocks.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

9/20/05

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100